Amendments to the Drawings:

The attached 2 sheets of drawings includes changes to Figs. 5A, 5B, and 5C. The attached 2 replacement sheets, which includes Figs. 5A, 5B, and 5C, replaces the original 2 sheets including Fig. 5A, 5B, and 5C.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Claims 1-4, 5-18, and 20-42 are pending. Claims 1, 3-4, 6-7, 11-12, 15, 17-18, 24, 27, 31, 35, and 39 are amended; and claims 5 and 19 are canceled.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5). FIGs. 5A, 5B, and 5C are amended to add the reference numerals 500a, 500b and 500c mentioned in the specification for the history buffer. The specification is amended to add reference numerals 309 and 331 in the related paragraph. In view of the amendments to the drawings and related amendments to the specification, it is respectfully requested that the above objections be withdrawn. The specification is also amended to correct typographical errors. No new matter is added.

Claims 11, 12, 18, 19, 24, 25, 27, 31, 35, and 39 are objected to because of informalities. In view of the amendments to the above claims, it is respectfully requested that the above objections be withdrawn.

Claims 1, 2, 8-16, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson et al. in view of Short et al. Claims 3-7, 17-21, and 27-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson et al. in view of Short et al., further in view of Yamaura. Applicants submit that all of the claims currently pending in this application are patentably distinguishable over the cited references, and reconsideration and allowance of this application are respectfully requested.

Amended independent claim 1 includes, among other limitations, "moving the second interrupt indicator associated with the younger control record onto the first interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data." None of the cited references, alone or in combination, teach or suggest the above limitation.

Pierson describes a Context Agile Encryption for high speed communication networks which "resembles ATM switches in that encryptors must retrieve information and make decision based on the cryptographic context associated with each VPI/VCI." (Section 2.0, first two lines of the last paragraph.). Pierson clearly states that the encyptor "transform[s] the incoming cell payload (plaintext or ciphertext) into the appropriate outgoing payload." (Section 2.0, lines 6-7 of the last paragraph.) A cell combiner combines data into a single high speed stream. The combiner may have three distinct implementation of a) FIFO queuing, b) latency matching with a constant and identical latency for all crypto paths, or c) a priority servicing, in which the "cell combiner must ensure that the cells are inserted into the cell stream in the same order as they were extracted, since ATM guarantees cell ordering." (Section 5.1.5, emphasis added.).

Therefore, there is no teaching or suggestion in Pierson about "moving the second interrupt indicator associated with the younger control record onto the first interrupt indicator associated with the older control record if processing of the

second data completes before processing of the first data," as recited by the amended claim 1.

Short describes a simple method for generating a single interrupt for a group of events. An interrupt controller "passes only a single interrupt request to the CPU 24 when a number of such interrupt events occur in a short time interval. The rate at which interrupts by the controlled peripheral device are permitted by the interrupt controller 50 is determined by two preset values, a limit and a delay time. The limit value sets a maximum number of pending interrupt events for the controlled peripheral device that the interrupt controller will allow to accumulate before asserting an IRQ to the CPU 24. The delay time value sets a maximum time interval that the interrupt controller will delay from the earliest pending interrupt event of the controlled peripheral device before asserting an IRQ to the CPU 24." (Col. 3, lines 53-64, underlining added.).

Accordingly, the purpose and function of the interrupt controller of short is different from the claimed invention. The claimed invention moves a second interrupt indicator onto a first interrupt indicator if processing of the second data completes before processing of the first data. In fact, by emphasizing that a single interrupt is generated based on number of pending interrupt events and maximum delay time interval, Short teaches away from "moving the second interrupt indicator . . . onto the first interrupt indicator . . . if processing of the second data completes before processing of the first data."

Applicants respectfully disagree with the statement in the Office action that Short in col. 4, lines 7-22 discloses moving

the first interrupt indicator on a second interrupt indicator. (Office action, page 10, last paragraph.). The cited text in Short simply disclose an interrupt event counter 60, a delay timer 62, a comparator 64 to implement the above discussed function, that is, generating an interrupt based on number of pending interrupt events and maximum delay time interval.

As a result, Short, alone or in combination with Pierson, does not teach or suggest the invention, as claimed by claim 1. Consequently amended claim 1 is patentable in view of the cited references.

Amended independent claim 15 includes a similar limitation of "wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record." Therefore, claim 15 is also patentable in view of Pierson/Short combination for the same reasons discussed above.

Amended independent claim 27 includes, among other limitations, "determining if any of the first or second interrupt indicators is enabled," and "if the second interrupt indicator is enabled and the processing of the first data block is not completed, generating a single interrupt upon completion of processing of the first data block."

Similarly, as explained above, by emphasizing that a single interrupt is generated based on number of pending interrupt events and maximum delay time interval, Short teaches away from "if the second interrupt indicator is enabled and the processing

of the first data block is not completed, generating a single interrupt upon completion of processing of the first data block." As a result claim 27 and claim 35, which includes similar limitation are also patentable in view of Pierson and Short.

In summary, independent claims 1, 15, 27, and 35 define a novel and unobvious invention over the cited references. Dependent claims 2-4, 6-14, 16-18, 20-26, 28-34, and 36-42 are dependent from claims 1, 15, 27 and 35, respectively and therefore include all the limitations of their respective independent claims and additional limitations therein. Accordingly, these claims are also allowable over the cited references, as being dependent from allowable independent claims and for the additional limitations they include therein.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
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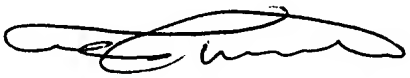
By 
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Fig. 5A

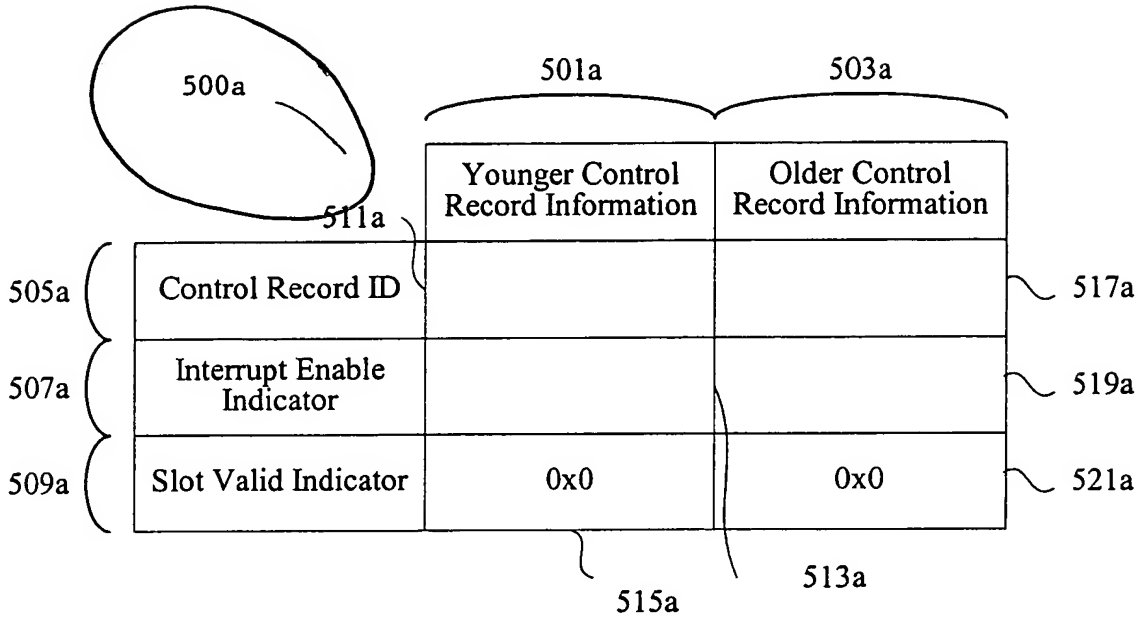

Fig. 5B

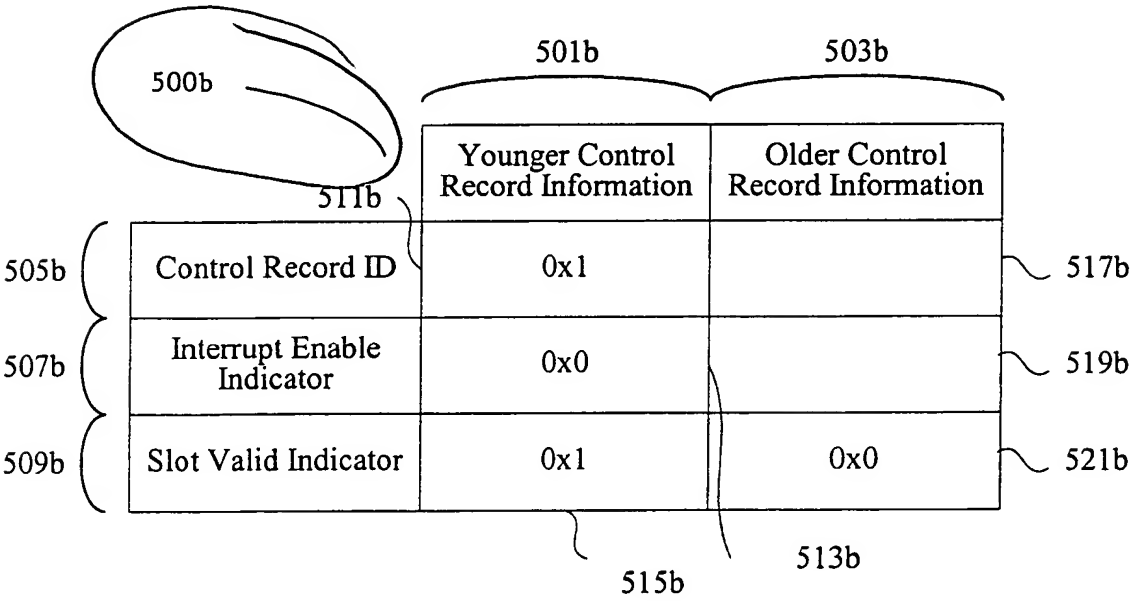

Fig. 5C

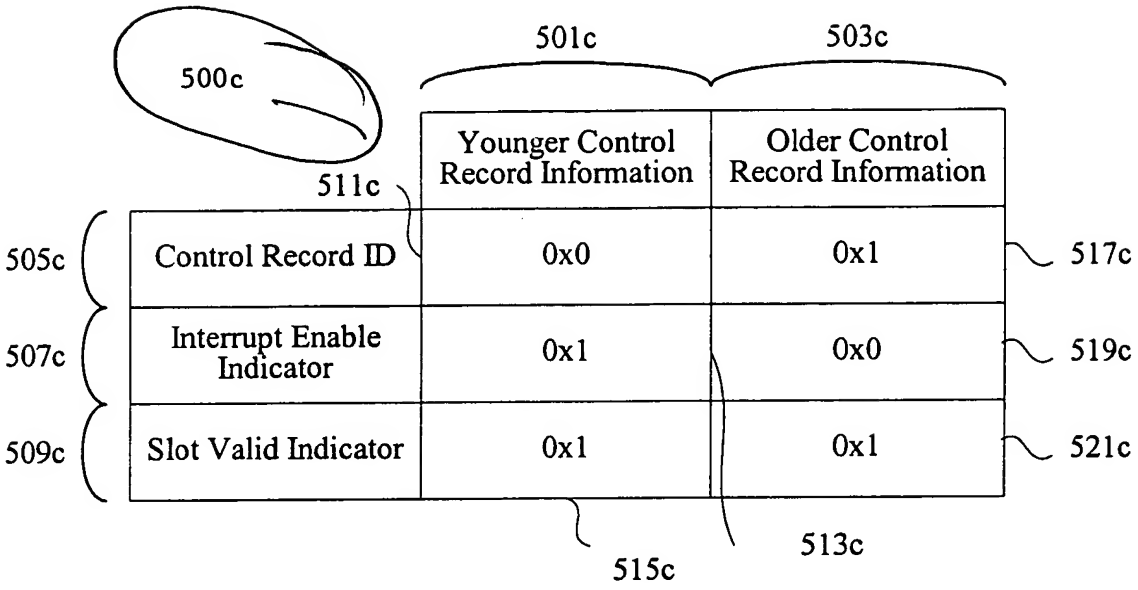

Fig. 5D